We Claim:

1. A method for forming a channel zone of a transistor below a polysilicon layer, which comprises:

patterning a polysilicon layer above the channel zone to be formed; and

subsequently doping the channel zone and using the patterned polysilicon layer as a mask substrate for doping the channel zone.

2. The method according to claim 1 configured for producing a PMOS field-effect transistor having a gate, a source, and a channel zone, the method which comprises the following steps:

(a) patterning the polysilicon layer to form holes in the gate region and to form pillars in the source region;

(b) doping the channel zone with a desired impurity concentration using the polysilicon layer patterned in step (a) as a doping mask; and

(c) outdiffusing the doped channel zone formed in step (b).

3. The method according to claim 2, which comprises choosing, in step (a), at least one of the parameters selected from the group consisting of form, spacing, number, and diameter of the

holes in the polysilicon in relation to at least one of the parameters selected from the group consisting of form, spacing, number, and diameter of the pillars in the source region such that, following outdiffusion in step (c), an impurity concentration of the channel zone in the source region is greater than an impurity concentration in the gate region.

4. In a PMOS field-effect transistor cell having a p-type channel zone below a polysilicon layer, the improvement which comprises:

the polysilicon layer having holes formed in a gate region and pillars formed in a source region, and wherein a p-type channel zone in the source region extends deeper into an n-type epitaxial layer than in the gate region and an impurity concentration of the p-type channel zone in the source region is greater than an impurity concentration of the p-type channel zone in the gate region.

5. The PMOS transistor cell according to claim 4 configured as a vertical depletion-mode MOS field-effect transistor cell.

6. The PMOS transistor cell according to claim 4 configured as a coolMOS™ cell.

7. The method according to claim 1 configured to serve for channel width shading of integrated PMOS transistor cells and having the following steps:

forming slots in sections of the polysilicon layer lying above the channel zone, to connect the channel zones of adjacent cells; and

introducing a p-type dopant into the slots in polysilicon, for electrically connecting the channel zones of mutually adjacent cells after the diffusion.

8. The method according to claim 7, choosing at least one of the parameters selected from the group consisting of position, form, spacing, number, width, and length of the slots or webs to achieve a desired channel width shading.

9. The method according to claim 1 configured to serve for channel width shading of an integrated PMOS transistor cell and having the following steps:

forming webs from the polysilicon within the polysilicon hole delimiting the source region, and short-circuiting the webs with the source electrode; and

utilizing the webs as masks during an implantation of the p-type dopant.

10. The method according to claim 7, choosing at least one of the parameters selected from the group consisting of position, form, spacing, number, width, and length of the slots or webs to achieve a desired channel width shading.

11. A PMOS transistor cell, comprising: a channel zone having a source region and a source electrode connected to said source region, a polysilicon layer lying above said channel zone, said polysilicon layer having slots or webs formed in sections thereof above said channel zone, said slots or webs being introduced to connect respective channel zones of adjacent transistor cells and said webs being residual portions of said polysilicon layer, lying within a polysilicon hole delimiting said source region, and being short-circuited with said source electrode.

12. The PMOS transistor cell as claimed in claim 11 formed as a vertical depletion-mode MOSFET transistor cell.